CLAIMS

1. A dynamic encoder for generating an N-bit encoder output word in response to each encoder input word of a sequence of encoder input words, where each encoder input word may represent any of N+1 different levels, where N is an integer greater than 4, the dynamic encoder comprising:

a plurality of switching blocks organized into a tree comprising at least a highest layer and a lowest layer of switching blocks,

wherein each switching block receives a block input word and converts it into R block output words, each of the R block output words having fewer bits than the block input word, such that a sum of values of the R block output words equals a value of the block input word, and such that when the value of the block input word is other than a multiple of R, a value of each one of its R block output words is other than solely a function of the value of the block input word,

wherein the highest layer of the tree includes a switching block receiving each successive encoder input word of the sequence as its block input word,

wherein each switching block of each layer of the tree other than the lowest layer supplies each of its R block output words as a block input word to a separate switching block of a next lower layer of the tree,

wherein each block output word of each switching block of the lowest layer of the tree consists of a single bit and forms a separate bit of the N-bit encoder output word,

wherein for at least one of the plurality of switching blocks R >2.

2. The dynamic encoder in accordance with claim 1 wherein for every switching block of every layer of the tree other than the highest layer of the tree R > 2.

3. The dynamic encoder in accordance with claim 1, wherein for at least one of the switching blocks R = 4.

4. The dynamic encoder in accordance with claim 3 wherein for every switching block R = 4.

5. The dynamic encoder in accordance with claim 1 wherein for at least one switching block R has a different value than for at least one other switching block.

6. The dynamic encoder in accordance with claim 1 wherein for at least one switching block R is other than a power of 2.

7. The dynamic encoder in accordance with claim 2

wherein N is a power of two other than a power of four, and

wherein for every switching block of every layer of the tree other than the highest layer of the tree R = 4.

8. The dynamic encoder in accordance with claim 1 wherein at least one switching block has a 2k+1 bit block input word and comprises:

a scrambling encoder for generating $R = 2^r$ scrambling encoder output bits in response to r least significant bits of the at least one switching block's block input word, wherein $r > 0$, wherein a sum of values of scrambling encoder output bits is equal to a value represented by the r least significant bits of the at least one switching block's block input word; and

R first summers, each corresponding to a separate one of the scrambling encoder output bits, each for generating a separate one of the at least one switching block's block R block output words as a sum of values of its corresponding scrambling encoder output bit and a 2k+1-r most significant bits of the at least one switching block's block input word.

9. The dynamic encoder in accordance with claim 1 wherein at least one switching block has a block input word z[n] and comprises:

a first circuit for producing data d[n] = MOD(z[n],R);

a second circuit for producing data q[n] = FLOOR(z[n]/R);

a scrambling encoder for generating R scrambling encoder output bits in response to data d[n], wherein a sum of values of scrambling encoder output bits is equal to a value represented by d[n]; and

R first summers, each corresponding to a separate one of the scrambling encoder output bits, each for generating a separate one of the at least one switching block's block R block output words as a sum of values of its corresponding scrambling encoder output bit and q[n].

10. The dynamic encoder in accordance with claim 8 wherein r >= 1

11. The dynamic encoder in accordance with claim 10 wherein r = 2.

12. The dynamic encoder in accordance with claim 8 wherein the scrambling encoder comprises:

a ranking circuit for monitoring the scrambling encoder output bits and for generating a plurality of ranking circuit output words as functions of past values of the scrambling encoder output bits, wherein each ranking circuit output word corresponds to a separate scrambling encoder output bit and wherein all ranking circuit output words have different values; and

a plurality of comparison circuits, each corresponding to a separate one of the ranking data words, each for generating a corresponding one of the scrambling encoder output bit of a value determined as a result of a comparison between its corresponding one of the ranking data words and a value of the r least significant bits of the at least one switching block's input data word.

13. The dynamic encoder in accordance with claim 12 wherein the ranking circuit comprises:

a plurality of second summers for generating a plurality of summer output words, each second summer corresponding to a separate one of the scrambling

encoder output bits other than a first scrambling encoder output bit and generating a summer output word representing a difference in values of its corresponding encoder output bit and the first scrambling encoder output bit,

a plurality of digital filters for separately filtering the separate summer output words to produce a plurality of filter output words; and

at least one comparator for generating the ranking circuit output words as functions of filter output words.

14. The dynamic encoder in accordance with claim 13 wherein each digital filter has a transfer function

$$F(z) = \frac{z^{-1}}{1 - z^{-1}}.$$

15. The dynamic encoder in accordance with claim 13 wherein each digital filter has a transfer function

$$F(z) = \frac{z^{-1}(2 - z^{-1})}{(1 - z^{-1})^2}.$$

16. A method for generating an N-bit encoder output word in response to each encoder input word of a sequence of encoder input words, wherein each encoder input word may represent any one of N+1 levels, where N is an integer greater than 4,

a. converting each encoder input word into a set of M generated words, each consisting of fewer bits than the encoder input word, wherein a sum of values of the M generated words equals a value of the encoder input word, and wherein M > 1; and

b. converting each previously generated word into a separate set of R generated words each consisting of fewer bits than the previously generated word, wherein combined values of the R generated words equals a value of the previously generated word, wherein values of the R generated words are other than sole functions of the previously generated word; and

c. iteratively executing step b until all generated words comprise only a single bit, wherein during each execution of step b, R>1, and wherein for at least one execution of step b, R>2.

17. The method in accordance with claim 18 wherein M >= 2.

18. The method in accordance with claim 17 wherein M = 4.

19. The method in accordance with claim 18 wherein R = 4 during each execution of step b.

20. The method in accordance with claim 16 wherein step b comprises for each previously generated word, the substeps of:

b1. generating $R = 2^r$ scrambling encoder output bits in response to r least significant bits of each previously generated word, wherein a sum of values of the scrambling encoder output bits equals a value represented by the r least significant bits of the previously generated output word, where r>0; and

b2. generating each word of the set of R generated words as a sum of a corresponding one of the scrambling encoder output bits and a 2k+1-r most significant bits of the previously generated word.

21 The method in accordance with claim 20 wherein r = 1.

22. The method in accordance with claim 20 wherein r = 2.

23. The method in accordance with claim 20 wherein substep b1 comprises the substeps of:

b11. monitoring the scrambling encoder output bits and generating a plurality of ranking data words as functions of past values of the scrambling encoder output

bits, wherein each ranking circuit output word corresponds to a separate scrambling encoder output bit and wherein all ranking data words have different values; and

b12. generating each one of the scrambling encoder output bits of a value determined as a result of a comparison between values of a corresponding one of the ranking data words and the r least significant bits of the previously generated output word.

24. The method in accordance with claim 23 wherein substep b11 comprises the substeps of:

b111. for each scrambling encoder output bit other than a first scrambling encoder output bit, generating a difference word sequence representing a difference in a sequence of values of the encoder output bit and a sequence of values of the first scrambling encoder output bit,

b112. digitally filtering a corresponding one of the difference words to sequence produce a separate filter output word sequence; and

b113. generating the ranking data words as functions of words of the filter output word sequences.

25. The method in accordance with claim 24 wherein difference word sequences are filtered at step b112 with a transfer function

$$F(z) = \frac{z^{-1}}{1 - z^{-1}}.$$

26. The method in accordance with claim 24 wherein difference word sequences are filtered at step b112 with a transfer function

$$F(z) = \frac{z^{-1}(2 - z^{-1})}{(1 - z^{-1})^2}.$$

27. A digital-to-analog converter (DAC) for generating an N+1 level analog DAC output signal in response to each DAC input word of a sequence of DAC input words, wherein each DAC input word may represent any of N+1 different levels, where N is an integer greater than 4, the DAC comprising:

a plurality of switching blocks organized into a tree comprising at least a highest layer and a lowest layer of switching blocks,

wherein each switching block receives a block input word and converts it into R block output words, each of the R block output words having fewer bits than the block input word, such that a sum of values of the R block output words equals a value of the block input word, and such that when the value of the block input word is other than a multiple of R, a value of each one of its R block output words is other than solely a function of the value of the block input word,

wherein the highest layer of the tree includes a switching block receiving each successive DAC input word of the sequence as its block input word,

wherein each switching block of each layer of the tree other than the lowest layer supplies each of its R block output words as a block input word to a separate switching block of a next lower layer of the tree,

wherein each block output word of each switching block of the lowest layer of the tree consists of a single bit,

wherein for at least one of the plurality of switching blocks $R > 2$;

a plurality of 1-bit DACs for converting the signal bit output words of switching blocks of the lowest layer of the tree into a plurality of analog signals; and

a summer for summing the plurality of analog signals to produce the analog DAC output signal.

28. The DAC in accordance with claim 27 wherein at least one switching block has a 2k+1 bit block input word and comprises:

a scrambling encoder for generating $R = 2^r$ scrambling encoder output bits in response to r least significant bits of the at least one switching block's block input word, wherein $r > 0$, wherein a sum of values of scrambling encoder output bits is equal to a

value represented by the r least significant bits of the at least one switching block's block input word; and

R first summers, each corresponding to a separate one of the scrambling encoder output bits, each for generating a separate one of the at least one switching block's block R block output words as a sum of values of its corresponding scrambling encoder output bit and a 2k+1-r most significant bits of the at least one switching block's block input word.

29. The DAC in accordance with claim 28 wherein the scrambling encoder comprises:

a ranking circuit for monitoring the scrambling encoder output bits and for generating a plurality of ranking circuit output words as functions of past values of the scrambling encoder output bits, wherein each ranking circuit output word corresponds to a separate scrambling encoder output bit and wherein all ranking circuit output words have different values; and

a plurality of first comparators, each corresponding to a separate one of the ranking data words, each for generating a corresponding one of the scrambling encoder output bit of a value determined as a result of a comparison between its corresponding one of the ranking data words and a value of the r least significant bits of the at least one switching block's input data word.

30. The DAC in accordance with claim 29 wherein the ranking circuit comprises:

a plurality of second summers for generating a plurality of summer output words, each second summer corresponding to a separate one of the scrambling encoder output bits other than a first scrambling encoder output bit and generating a summer output word representing a difference in values of its corresponding encoder output bit and the first scrambling encoder output bit,

a plurality of digital filter for separately filtering the separate summer output words to produce a plurality of filter output words; and

at least one second comparator for generating the ranking circuit output words as functions of filter output words.

31. The DAC in accordance with claim 30 wherein each digital filter has a transfer function

$$F(z) = \frac{z^{-1}}{1 - z^{-1}}.$$

32. The DAC in accordance with claim 30 wherein each digital filter has a transfer function

$$F(z) = \frac{z^{-1}(2 - z^{-1})}{(1 - z^{-1})^2}.$$

33. The DAC in accordance with claim 27 wherein at least one switching block has a block input word z[n], where n is a discrete time index, and comprises:

a first circuit for producing data d[n] = MOD(z[n],R);

a second circuit for producing data q[n] = FLOOR(z[n]R);

a scrambling encoder for generating R scrambling encoder output bits in response to values of data d[n], wherein a sum of values of scrambling encoder output bits is equal to a value represented by data d[n]; and

R first summers, each corresponding to a separate one of the scrambling encoder output bits, each for generating a separate one of the at least one switching block's block R block output words as a sum of values of its corresponding scrambling encoder output bit and q[n].